REMARKS

Claims 1-24 are pending in the application. Claims 1, 8, 13, 17 and 22 have been amended.

Claim Rejections – 35 U.S.C. §102(b)

The Examiner rejected claims 1-5, 7-10, 12-14, 17-20, 22 and 24 under 35 USC 102(e) as being anticipated by Devic (U.S. Patent No. 6,054,993). Applicant respectfully disagrees with the Examiner's rejection. In particular, Devic fails to teach or suggest a "logical binding is provided between the internal texture coordinate sets used by the graphics device and plurality of texture coordinates associated with vertices of three dimensional objects," as claimed in independent claims 1, 8, 13, 17, 22 and the claims that depend therefrom.

The present invention provides a logical binding between the *internal* texture coordinate sets used by a graphics device and *externally* stored (i.e., within the system memory) vertex texture coordinates or a default value. This logical mapping provides substantial flexibility with respect to the use, ordering and possibly replication of vertex texture coordinates. As noted in the specification on page 11, line 7 to page 12, line 2:

> Accordingly, by utilizing these logical bindings, specific vertex texture coordinate sets that are present in the vertex data array may be ignored. This may better support the operation of the Direct 3D API, which does not prevent unused texture coordinate sets from being presented to the graphics driver or stored in the vertex buffers. This allows applications to keep one vertex database (with possibly more texture coordinates sets than the hardware can use at any point in time) and then employ a multipass rendering algorithm where a subset of the coordinate sets may be used in each pass.
>
> The logical binding functionality may allow multiple internal texture coordinate sets to be bound to the same vertex texture coordinate sets. This may be useful for replicating vertex texture coordinate sets in order to apply different attributes (e.g., texture address controls, texture coordinate transforms, etc.) to the same texture coordinate set for use with different texture mappings. This may be useful for matching the Direct 3D API semantics of associating these controls with texture stages versus texture coordinate sets.
>
> The logical bindings also allow the vertex texture coordinate sets to be used in a random (versus strictly sequential) fashion.
>
> Embodiments of the present invention provide advantages over graphic devices that support a fixed (i.e., implied) binding between the vertex texture coordinate set and the internal texture coordinate sets. That is, embodiments of

the present invention permit vertex texture coordinates to be ignored, permit vertex texture coordinates to be replicated, permit vertex texture coordinates to be used in random order and permit the association of a default value to a texture coordinate set. Without this flexibility, the graphics driver would be generate a second, rearranged copy of the vertex data, which adds additional memory bandwidth requirements and software overhead and thus reduces the system performance.

Devic fails to teach or suggest a logical binding that provided between the internal texture coordinate sets used by the graphics device and plurality of texture coordinates associated with vertices of three dimensional objects. In fact, Devic teaches away in that it supports a fixed (i.e. implied) binding between vertex and internal texture coordinate sets. This requires the graphics driver to generate a second, rearranged copy of the vertex data (adding software overhead and thus reducing system performance).

It is therefore respectfully requested that the Examiner withdraw his rejection of the pending claims.

Claim Rejections – 35 U.S.C. §103

Claims 6, 11, 15, 18, 21 and 23 are patentable over Devic for the same reasons noted above.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

The required fee for a one month extension of time is enclosed. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, she is invited to contact the undersigned at (310) 252-7605. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

Dated: December 29, 2003

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Fee Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on December 31, 2003.

Margaux Rodriguez *December 31, 2003*